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Smart Grid Voltage Synchronization for Distributed Generation Systems Under Grid Fault Conditions for Automation Systems

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Abstract

The assimilation of Distributed Generation (DG) systems into smart grids introduces challenges in maintaining voltage synchronization, particularly under grid fault conditions. This paper investigates advanced control strategies for voltage synchronization in DG systems to ensure stable operation during faults, enhancing grid resilience and automation. A new synchronization method is suggested that makes use of fault-ride-through (FRT) and adaptive Phase-Locked Loop (PLL) capabilities. Simulation results using MATLAB/Simulink demonstrate the efficiency of the proposed method in maintaining synchronization and improving quality of power under various fault scenarios.

Keywords: Smart Grid, Distributed Generation (DG), Voltage Synchronization, Phase-Locked Loop (PLL), Fault-Ride-Through (FRT), Automation Systems

I. INTRODUCTION

Maintaining voltage synchronization has become more difficult as a result of the quick integration of Distributed Generation (DG) systems, such as solar PV, wind turbines, and energy storage, into contemporary smart grids, especially in the event of a grid failure. [1]. Synchronization is critical to ensure stable power exchange between DG units and the main grid, but faults (e.g., voltage sags, swells, phase jumps, and asymmetrical faults) can disrupt this process, leading to instability, protection tripping, and even blackouts [2]. Traditional synchronous generators inherently maintain grid synchronization due to their rotating inertia. However, inverter-based DG systems rely on Phase-Locked Loops (PLLs) for synchronization, making them vulnerable to grid disturbances [3]. When a fault occurs, conventional PLLs (e.g., Synchronous Reference Frame PLL) may fail to track the grid voltage accurately, leading to Loss of synchronization (causing DG disconnection), Increased

harmonic distortion and Cascading failures in automated protection systems [4]. To enhance Fault-Ride-Through (FRT) capability, advanced synchronization techniques must be developed to ensure seamless operation under fault conditions, supporting smart grid automation and microgrid resilience [5]. Several methods have been proposed to improve PLL performance under faults. Dual Second-Order Generalized Integrator (DSOGI-PLL) – Robust against unbalanced faults but suffers from slow dynamic response [6]. Enhanced SRF-PLL with adaptive filters – Improves harmonic rejection but lacks fast fault detection [7]. Machine Learning-based PLLs – Emerging but require extensive training data [8]. Despite these advancements, real-time adaptive synchronization remains a challenge, particularly for automated grid recovery systems that require millisecond-level corrections [9]-[12]. This paper proposes an adaptive PLL-based synchronization strategy with:

- Dynamic bandwidth adjustment to handle voltage sags/swells.
- Fault detection and mode-switching logic for rapid response.
- Virtual impedance control to enhance FRT capability.

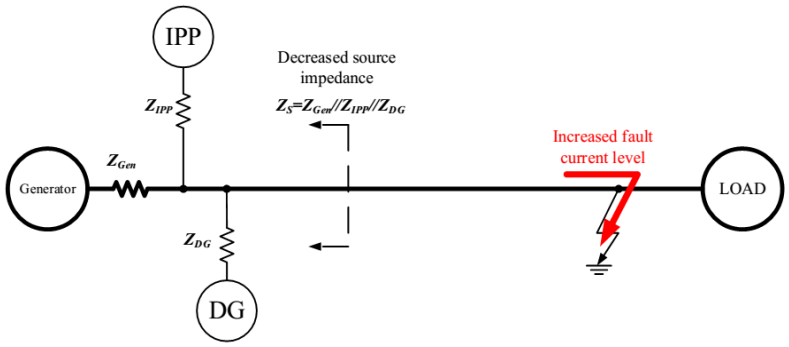


Figure 1:Parallel IPP and DG decrease source impedance and increase potential fault current level on the power system

The proposed method is validated through MATLAB/Simulink simulations under various fault scenarios, demonstrating superior performance compared to conventional approaches. Section 2 reviews synchronization challenges in DG systems. Section 3 presents the proposed adaptive PLL design. Simulation results are discussed in Section 4. Conclusion with key findings and future work in Section 5.

II. PROBEM STATEMENT

When a grid fault occurs, conventional synchronization methods (e.g., SRF-PLL) may fail due to Voltage magnitude variations, Frequency deviations, Phase-angle jumps. This leads to:

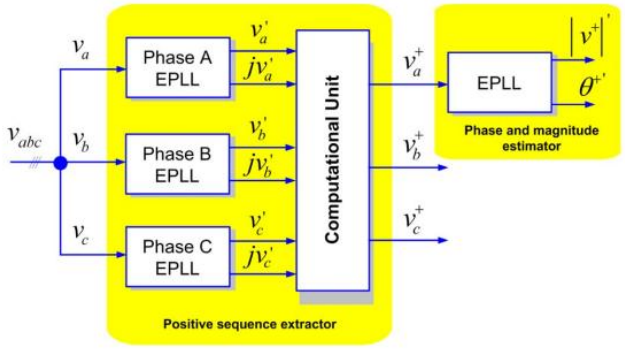
- Loss of DG synchronization.
- Cascading failures in automation systems.
- Reduced grid stability.

An adaptive synchronization mechanism is needed to ensure continuous operation under fault conditions. Proposed Solution Adaptive PLL with Fault-Ride-Through (FRT) Capability, The proposed method combines: Enhanced SRF-PLL with Adaptive Filtering, Enhanced SRF-PLL with Adaptive Filtering Uses a dynamic low-pass filter to eliminate harmonics during faults. Adjusts bandwidth based on grid disturbance severity. Fault Detection and Mode Switching for Real-time fault detection using RMS voltage monitoring. Switches between normal and fault modes to maintain synchronization. Virtual Impedance Control, which Enhances fault-ride-through capability by injecting reactive power to stabilize voltage.

III. Advanced Mathematical Formulation of Adaptive PLL with FRT Capability

One synchronization method that has shown promise in single phase synchronization systems is the enhanced phase-locked loop (EPLL) . An EPLL is essentially an adaptive bandpass filter, which is able to adjust the cutoff frequency as a function of the input signal. In order to identify the positive-sequence vector of three-phase signals, its structure was later modified for the three-phase situation, yielding the 3phEPLL shown in Fig. 2. An EPLL processes each phase voltage separately in this instance. The input signal is filtered by this block, which then produces two sinusoidal outputs with the same amplitude and frequency (vn and j_{vn}), the second of which is 90◦ with respect to vn. The signals that are produced serve as the computing unit's input. Due to these in-quadrature signals, the positive-sequence voltage component, $v_{abc}+$ that occurs instantly, can be estimated by means of using the ISC method. Since the continuous representation of multiple components remains unchanged in the discrete domain, the discrete model of this PLL may be derived with ease. The broad scope literature describes the transformation blocks Tαβ, Tdq+1, and Tdq−1, and this is the case for them.

1) **Positive and Negative-Sequence Decoupling Networks:** The decoupling network constitutes one of the most important contributions of this synchronization method. The discrete equations of these blocks are shown in (1), being almost the same as in the continuous domain. To prevent algebraic loops, one sample delay of θ, v¯d−1, v ¯q−1, v ¯d+1, and v ¯q+1 must be taken into account.
2) **Phase and Magnitude Estimator Discretization:** Fig. 3.6 shows the decoupling network included in the classical SRF-PLL loop in the DDSRF PLL. The discretization of the phase and magnitude estimator is unaffected by this, though, because v∗d+1 and vq∗+1 serve as this block's inputs.



3)

Figure 2:3phEPLL block diagram.

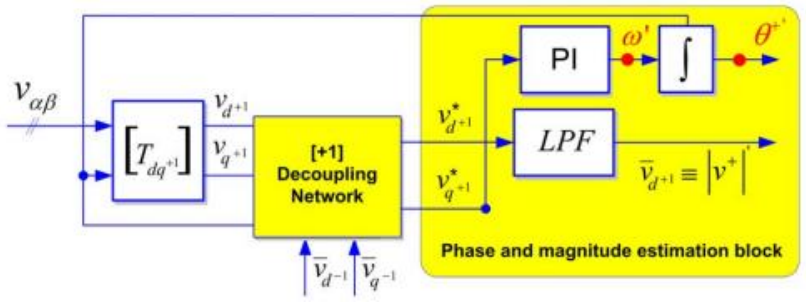


Figure 3:Phase and magnitude estimation loop of the DDSRF PLL.

A. Enhanced SRF-PLL with Adaptive Filtering

i) Modified SRF-PLL Structure

The enhanced PLL architecture incorporates an adaptive filtering stage before the conventional SRF-PLL:

$v_{\alpha\beta} = T_{abc} \rightarrow \alpha\beta \cdot v_{abc}$ (1)

$v_{\alpha\beta} - filt = H(s) \cdot v_{\alpha\beta}$ (2)

$v_{dq} = T_{\alpha\beta} \rightarrow dq(\theta_{est}) \cdot v_{\alpha\beta - filt}$ (3)

where:

$T_{abc} \rightarrow \alpha\beta$ = Clarke transformation matrix

$T_{\alpha\beta} \rightarrow dq$ = Park transformation matrix

θ_{est} = Estimated phase angle

ii) Adaptive Filter Dynamics

The time-varying low-pass filter is implemented as:

$H(s,t) = \omega_c(t)/(s + \omega_c(t))$ (4)

with the cutoff frequency adaptation law:

$\omega_c(t) = \omega_{c0} + K_f \cdot e_v(t)$ (5)

$e_v(t) = |V_rms(t) - V_nom|/V_nom$ (6)

where:

$\omega_{c0} = 2\pi \cdot 25 rad/s$ (nominal cutoff)

$K_f = 2\pi \cdot 100 rad/s$ per pu voltage deviation

iii) Bandwidth Adaptation Mechanism

The PI controller gains are made adaptive through:

$K_p(t) = 2\zeta\alpha(t)$ (7)

$K_i(t) = \alpha^2(t)$ (8)

with the bandwidth adjustment:

$\alpha(t) = \alpha_{min} + (\alpha_{max} - \alpha_{min}) \cdot S(e_v(t))$ (9)

where S(x) is a sigmoidal function:

$S(x) = 1/(1 + e^{(-k(x-x_0))})$ (10)

Typical parameters:

$\alpha_{min} = 2\pi \cdot 5 rad/s$

$\alpha_{max} = 2\pi \cdot 50 rad/s$
$k = 20, x_0 = 0.1pu$

B. Fault Detection and Mode Switching

i) RMS Voltage Calculation

The moving-window RMS computation:

$$V_rms(t) = \sqrt{\left(1/T_w \int (t - T_w)^t v_\alpha^2(\tau) + v_\beta^2(\tau) d\tau\right)} \quad (11)$$

where $T_w = 1/4$ cycle window (5 ms for 50 Hz).

ii) Fault Declaration Logic

Fault condition is triggered when:

$$Fault\_flag = \{ 1,\ V_{rms}(t) < V_{th}\ and\ dV_{rms}/dt > R_{th}\ , \quad 0, otherwise \} \quad (12)$$

where:

$V_{th} = 0.85pu$
$R_{th} = 0.5pu/s$

iii) Mode Transition Dynamics

The system switches between normal (N) and fault (F) modes following:

$$dx_{mode}/dt = -\tau_m^{-1} \quad (x_{mode} - x_{desired}) \quad (13)$$

where:

$x_{mode} \in [0,1]$ (0 = normal, 1 = fault)
τ_m = 5 ms (transition time constant)

IV. Virtual Impedance Control

A. Current Reference Modification

The virtual impedance modifies current references as:

$$[i_d^{ref}] = [R_v X_v][i_d] + [i_{d0}] \quad (14)$$
$$[i_q^{ref}] = [-X_v R_v][i_q] + [i_{q0}] \quad (15)$$

where:

$R_v = 0.2pu$
$X_v = 0.4pu$
i_{d0}, i_{q0} = Pre-fault current references

ii) Dynamic Impedance Adjustment

The virtual impedance parameters adapt via:

$$\mathrm{R_v(t)} = \mathrm{R_v0} \cdot \left(1 + K_R \cdot (1 - V_{rms}(t)/V_{nom})\right)$$
$$X_v(t) = X_v0 \cdot \left(1 + K_X \cdot (1 - V_{rms}(t)/V_{nom})\right) \quad (16)$$

with:

$R_{v0} = 0.1pu, K_R = 1.5$
$X_{v0} = 0.2pu, K_X = 1.0$

B. *Performance Metrics*

i) Synchronization Accuracy : It is a measure of PLL error and it is estimated as,
Phase locking error bound:

$$|\Delta\theta| < \Delta\theta_{max} = \alpha^{-1} \cdot (\omega_{max} + K_p \cdot V_{harm})$$

where:

ω_{max} = maximum frequency deviation

V_{harm} = harmonic content

ii) Dynamic Response

Settling time for 98% convergence:

$$t_s \approx 4/(\zeta\alpha(t))$$

C. *Discrete-Time Implementation*

The digital implementation uses:

$$\omega_c[k] = \omega_{c0} + K_{f.e}v[k]$$

$$H(z) = (T_s\omega_c[k])/(1 + T_s\omega_c[k] - z^{-1})$$

where T_s is the sampling period.

V. RESULTS & DISCUSSION

The Simulink Diagram of the proposed system is shown below:

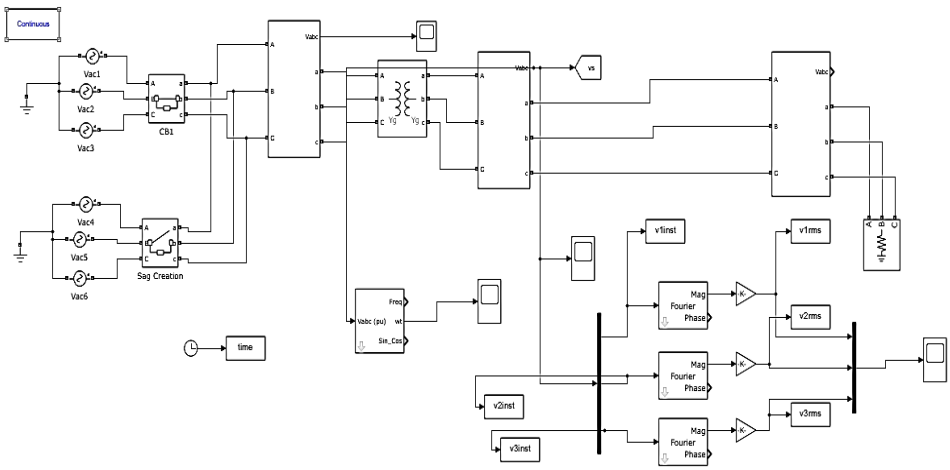


Figure 4: Simulink Implementation of Proposed system

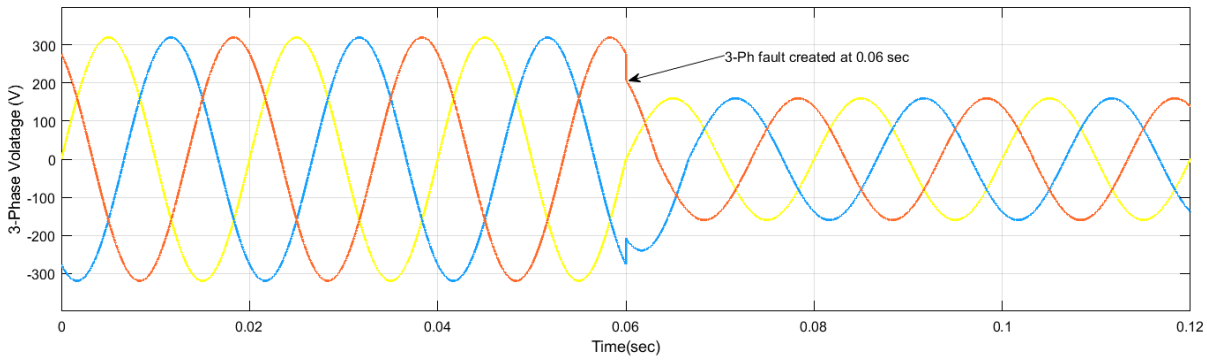


Figure 5: 3-phase voltage waveform with a symmetrical fault occur at 0.06 sec

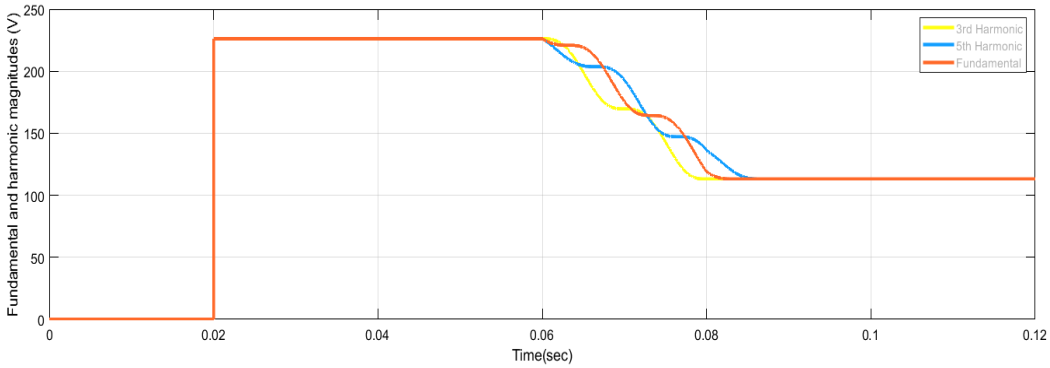


Figure 6:Magnitudes of Harmonics after occurrence of 3-phase Fault

VI. CONCLUSION

The proposed system evaluated three advanced synchronization techniques—DDSRF-PLL, DSOGI-PLL, and 3phEPLL—for grid-tied distributed generation systems. Experimental validation on a DSP platform demonstrated that all three methods achieve fast (20–25 ms) and accurate positive-sequence detection under faults and harmonic distortion. While the 3phEPLL offers superior harmonic immunity due to enhanced filtering, the DDSRF-PLL and DSOGI-PLL provide a better trade-off, combining lower computational burden (αβ-frame operation) with robust performance. Their simpler tuning and transient response control make them particularly suitable for wind/PV applications, where real-time efficiency is critical. For highly distorted grids, the 3phEPLL remains preferable, though at higher computational cost. The choice depends on grid conditions and implementation constraints.

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